REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Drawings

Figure 1 has been objected to for not including the legend Prior Art. Figure 1 has been amended to include the legend and a replacement sheet is being submitted herewith.

Claim Rejections - 35 USC § 112

Claims 7-10 and 16-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Applicants respectfully traverse these rejections.

The Examiner has stated that "[c]laims 7 and 16 recite the limitation "a second clock modifier ..." This limitation is not disclosed in the specification." Applicants respectfully disagree. Applicants would like to respectfully point to the Examiner that specification clearly defines the second clock modifier. In figures 3, 4A, and 4B and corresponding description, a second clock modifier NCO 210 and its function are described. As described on pages 11-12, NCO 210 introduces clock jitter equivalent to the maximum jitters introduced by the delay line 310, which allows the introduction of delays indefinitely. Accordingly, the specification clearly describes the subject matter recited in claims 7 and 16.

Similarly, as described above, NCO 210 introduces clock jitter that is equivalent to a predetermined plurality of tapped phase delays (*see* page 11, line17 – page 12, line 2). Therefore, the subject matter of claims 10 and 18 is also adequately described in the specification.

Accordingly, applicants respectfully request the withdrawal of the rejection of claims 7-10, and 16-18 under 35 USC §112, first paragraph.

Claim Rejections - 35 USC §102

Claims 1-6 and 11-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kovacs et al (5,646,968). Applicants respectfully traverse these rejections.

To anticipate a claim under 35 USC §102(b), the reference must teach every element of the claim. *See* MPEP §2131. Kovacs et al. do not teach each and every limitation of claim 1.

As to claim 1, the Examiner has cited elements 26 and 28 as phase estimators. Applicants respectfully point to the Examiner that elements 26 and 28 do not determine a phase error with respect to a remote clock and a local clock as recited in claim 1. According to Kovacs et al., element 26 "determines the amount of phase error, if any, in the sampling of the input signal **by comparing** the level of the input signal sampled **to the correct, desired sampling level**, i.e., **+1 or -1**." (Col. 4, lines 24-28, emphasis added). Thus, the comparison is done based on a predetermined desired level and not with respect to a local clock signal as recited in claim 1.

Further, according to Kovacs et al., the phase detector 26 receives predetermined input as shown and described with reference to figures 4 and 6. Each deviation is predetermined to be around +/- 30 degrees and the output signal is chosen from the look-up table 174 accordingly. Thus, Kovacs et al. do not teach determining a phase error with respect to a remote clock signal and a local clock signal as recited in claim 1.

Furthermore, as to the first clock modifier as recited in claim 1, the Examiner has cited the elements 42 and 30 of Kovacs et al. Applicants respectfully point to the Examiner that claim 1 recites a first clock modifier having an input for receiving said local clock signal and operable to apply a first phase modifier responsive to said issued correction signal, said first clock modifier further having an output for issuing **a synchronized clock signal**. The elements cited by the Examiner do not receive a local clock signal as recited in claim 1. The phase selector 42 receives input only from a phase detector 26 and frequency detector 34 and outputs signals to the loop filter 28, VCO 30, and Gate 43. It does not receive a local clock signal as the first clock modifier in claim 1. Accordingly, Kovacs et al. do not teach each and every limitation of claim 1 and claim 1 is patentably distinguishable from Kovacs et al.

Claim 11 has been rejected in the manner of claim1. Accordingly, claim 11 is patentably distinguishable from Kovacs et al. for at least the same reasons as claim 1.

Claim 2 depends from claim 1 and is patentably distinguishable from Kovacs et al. for at least the same reasons as claim 1.

Claims 3 and 12 depend from claims 1 and 11 respectively and are patentably distinguishable from Kovacs et al. for at least the same reasons as claims 1 and 11.

Claims 4 and 13 depend from claims 1 and 11 respectively and are patentably distinguishable from Kovacs et al. for at least the same reasons as claims 1 and 11. Further, as to claims 4 and 13, the Examiner has cited figure 4 of Kovacs et al. Applicants respectfully point to the Examiner that in figure 4, Kovacs et al. actually describes the delay tap adjustment signals that can be generated in response to possible phase error signals (*see* col. 6, lines 38-43). When the phase selector circuit 42 of Kovacs et al. receives a phase error signal, then the phase error signal is provided to the look-up table 174, which outputs appropriate delay tap adjustment and the delay tap adjustment is then provided to VCO 30 (*see* col. 7, lines 15-29). Accordingly, Kovacs. Et al. does not apply jitters to **local clock signal** in equal distribution over a time period as recited in claims 4 and 13. Accordingly, claims 4 and 13 are further patentably distinguishable from Kovacs et al.

Claims 5 and 14 depend from claims 1 and 11 respectively and are patentably distinguishable from Kovacs et al. for at least the same reasons as claims 1 and 14.

As to claims 6 and 15, applicants respectfully request a careful reading of these claims. Claims 6 and 15 recite that **first clock modifier further includes** a **phase selector** having an **input for receiving** a **tapped coupling from each of said delay elements**, **a serial coupling of all delay elements**, and **said local clock signal**, wherein said phase selector is further operable to select a clock jitter responsive to said issued correction signal. The Examiner has not cited any element, which includes elements as recited in claims 6 and 15. In rejecting claim 1, the Examiner cited elements 42 and 32 as the first clock modifier and a careful reading of the cited sections in Kovacs et al. reveal that these elements do not have inputs for receiving taped coupling from delay elements. In fact, figure 3 clearly shows that the tapped couplings are only

provided to a gate 43 in the form of a clock signal. Further, these elements do not receive a local clock signal as recited in claims 6 and 13. Accordingly, Kovacs et al. do not teach each and every limitation of claims 6 and 13 as required to anticipate under 35 USC §102(b) and claims 6 and 13 are patentably distinguishable from Kovacs et al.

As to claims 7-10 and 16-18, the Examiner has not issued any substantive rejection thus Applicants believe that these claims are patentably distinguishable from Kovacs et al.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

Abdul Zindani
Attorney for Applicant
Reg. No. 46,091

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5137